## Dual 12MHz Rail-to-Rail Input-Output Buffer

The EL5221 is a dual, low power, high voltage rail-to-rail input-output buffer. Operating on supplies ranging from 5V to 15V, while consuming only 500µA per channel, the EL5221 has a bandwidth of 12MHz (-3dB). The EL5221 also provides rail-to-rail input and output ability, giving the maximum dynamic range at any supply voltage.

The EL5221 also features fast slewing and settling times, as well as a high output drive capability of 30mA (sink and source). These features make the EL5221 ideal for use as voltage reference buffers in Thin Film Transistor Liquid Crystal Displays (TFT-LCD). Other applications include battery power, portable devices, and anywhere low power consumption is important.

The EL5221 is available in space-saving 6 Ld SOT-23 and 8 Ld MSOP packages and operates over a temperature range of -40°C to +85°C.

## Ordering Information

| PART NUMBER | PART MARKING | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| EL5221CW-T7* | M | 6 Ld SOT-23 | MDP0038 |
| EL5221CW-T7A* | M | 6 Ld SOT-23 | MDP0038 |
| EL5221CWZ-T7* (Note) | BBEA | 6 Ld SOT-23 (Pb-free) | MDP0038 |
| EL5221CWZ-T7A* (Note) | BBEA | 6 Ld SOT-23 (Pb-free) | MDP0038 |
| EL5221CY | K | 8 Ld MSOP | MDP0043 |
| EL5221CY-T7* | K | 8 Ld MSOP | MDP0043 |
| EL5221CY-T13* | K | 8 Ld MSOP | MDP0043 |
| EL5221CYZ (Note) | BAAAJ | 8 Ld MSOP (Pb-free) | MDP0043 |
| EL5221CYZ-T7* (Note) | BAAAJ | 8 Ld MSOP (Pb-free) | MDP0043 |
| EL5221CYZ-T13* (Note) | BAAAJ | 8 Ld MSOP (Pb-free) | MDP0043 |

*Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

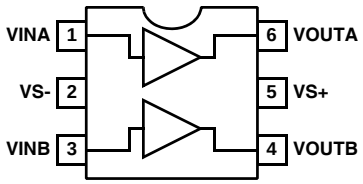
- 12MHz -3dB bandwidth
- Unity gain buffer
- Supply voltage = 4.5V to 16.5V
- Low supply current (per buffer) = 500µA
- High slew rate = 10V/µs
- Rail-to-rail operation
- Pb-Free plus anneal available (RoHS compliant)

## Applications

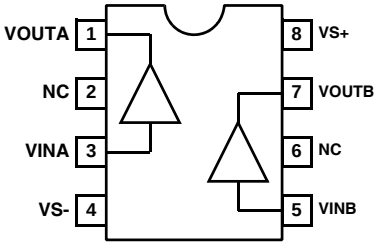
- TFT-LCD drive circuits
- Electronics notebooks
- Electronics games
- Personal communication devices
- Personal Digital Assistants (PDA)
- Portable instrumentation
- Wireless LANs
- Office automation
- Active filters
- ADC/DAC buffer

## Pinouts

**EL5221**
**(6 LD SOT-23)**
**TOP VIEW**




**EL5221**
**(8 LD MSOP)**
TOP VIEW



## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply Voltage between $V_S$+ and $V_S$- . . . . . .+18V
Input Voltage . . . . . $V_S$- - 0.5V, $V_S$+ +0.5V
Maximum Continuous Output Current . . . . . 30mA
ESD Voltage. . . . . .2kV

## Thermal Information

Storage Temperature . . . . . .-65°C to +150°C
Operating Temperature . . . . . .-40°C to +85°C
Power Dissipation . . . . . See Curves
Maximum Die Temperature . . . . . .+125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

## Electrical Specifications

$V_S$+ = +5V, $V_S$- = -5V, $R_L$ = 10kΩ and $C_L$ = 10pF to 0V, $T_A$ = +25°C unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITION | MIN (Note 3) | TYP | MAX (Note 3) | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = 0V | | 2 | 12 | mV |
| $TCV_{OS}$ | Average Offset Voltage Drift | (Note 1) | | 5 | | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM}$ = 0V | | 2 | 50 | nA |
| $R_{IN}$ | Input Impedance | | | 1 | | GΩ |
| $C_{IN}$ | Input Capacitance | | | 1.35 | | pF |
| $A_V$ | Voltage Gain | -4.5V ≤ $V_{OUT}$ ≤ 4.5V | 0.995 | | 1.005 | V/V |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OL}$ | Output Swing Low | $I_L$ = -5mA | | -4.92 | -4.85 | V |
| $V_{OH}$ | Output Swing High | $I_L$ = 5mA | 4.85 | 4.92 | | V |
| $I_{SC}$ | Short Circuit Current | Short to GND | | ±120 | | mA |
| **POWER SUPPLY PERFORMANCE** | | | | | | |
| PSRR | Power Supply Rejection Ratio | $V_S$ is moved from ±2.25V to ±7.75V | 60 | 80 | | dB |
| $I_S$ | Supply Current (Per Buffer) | No load | | 500 | 750 | µA |
| **DYNAMIC PERFORMANCE** | | | | | | |
| SR | Slew Rate (Note 2) | -4.0V ≤ $V_{OUT}$ ≤ 4.0V, 20% to 80% | 7 | 10 | | V/µs |
| $t_S$ | Settling to +0.1% | $V_O$ = 2V step | | 500 | | ns |
| BW | -3dB Bandwidth | $R_L$ = 10kΩ, $C_L$ = 10pF | | 12 | | MHz |
| CS | Channel Separation | f = 5MHz | | 75 | | dB |

**Electrical Specifications** $V_S+ = +5V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 2.5V, $T_A = +25°C$ unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITION | MIN (NOTE 3) | TYP | MAX (NOTE 3) | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | $V_{CM} = 2.5V$ | | 2 | 10 | mV |
| $TCV_{OS}$ | Average Offset Voltage Drift | (Note 1) | | 5 | | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM} = 2.5V$ | | 2 | 50 | nA |
| $R_{IN}$ | Input Impedance | | | 1 | | GΩ |
| $C_{IN}$ | Input Capacitance | | | 1.35 | | pF |
| $A_V$ | Voltage Gain | $0.5 \le V_{OUT} \le 4.5V$ | 0.995 | | 1.005 | V/V |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OL}$ | Output Swing Low | $I_L = -5mA$ | | 80 | 150 | mV |
| $V_{OH}$ | Output Swing High | $I_L = 5mA$ | 4.85 | 4.92 | | V |
| $I_{SC}$ | Short Circuit Current | Short to GND | | ±120 | | mA |
| **POWER SUPPLY PERFORMANCE** | | | | | | |
| PSRR | Power Supply Rejection Ratio | $V_S$ is moved from 4.5V to 15.5V | 60 | 80 | | dB |
| $I_S$ | Supply Current (Per Buffer) | No Load | | 500 | 750 | µA |
| **DYNAMIC PERFORMANCE** | | | | | | |
| SR | Slew Rate (Note 2) | $1V \le V_{OUT} \le 4V$, 20% to 80% | 7 | 10 | | V/µs |
| $t_S$ | Settling to +0.1% | $V_O = 2V$ Step | | 500 | | ns |
| BW | -3dB Bandwidth | $R_L = 10k\Omega$, $C_L = 10pF$ | | 12 | | MHz |
| CS | Channel Separation | f = 5MHz | | 75 | | dB |

**Electrical Specifications** $V_S+ = +15V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 7.5V, $T_A = +25°C$ unless otherwise specified.

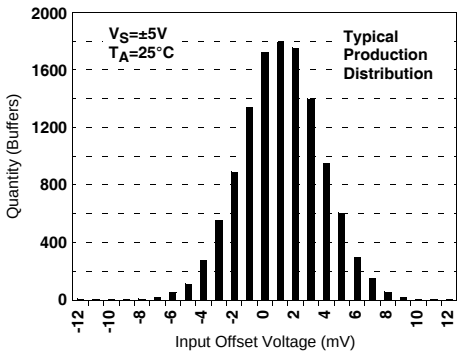
| PARAMETER | DESCRIPTION | CONDITION | MIN (NOTE 3) | TYP | MAX (NOTE 3) | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | $V_{CM} = 7.5V$ | | 2 | 14 | mV |
| $TCV_{OS}$ | Average Offset Voltage Drift | (Note 1) | | 5 | | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM} = 7.5V$ | | 2 | 50 | nA |
| $R_{IN}$ | Input Impedance | | | 1 | | GΩ |
| $C_{IN}$ | Input Capacitance | | | 1.35 | | pF |
| $A_V$ | Voltage Gain | $0.5 \le V_{OUT} \le 14.5V$ | 0.995 | | 1.005 | V/V |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OL}$ | Output Swing Low | $I_L = -5mA$ | | 80 | 150 | mV |
| $V_{OH}$ | Output Swing High | $I_L = 5mA$ | 14.85 | 14.92 | | V |
| $I_{SC}$ | Short Circuit Current | Short to GND | | ±120 | | mA |
| **POWER SUPPLY PERFORMANCE** | | | | | | |
| PSRR | Power Supply Rejection Ratio | $V_S$ is moved from 4.5V to 15.5V | 60 | 80 | | dB |
| $I_S$ | Supply Current (Per Buffer) | No Load | | 500 | 750 | µA |
| **DYNAMIC PERFORMANCE** | | | | | | |
| SR | Slew Rate (Note 2) | $1V \le V_{OUT} \le 14V$, 20% to 80% | 7 | 10 | | V/µs |
| $t_S$ | Settling to +0.1% | $V_O = 2V$ Step | | 500 | | ns |
| BW | -3dB Bandwidth | $R_L = 10k\Omega$, $C_L = 10pF$ | | 12 | | MHz |
| CS | Channel Separation | f = 5MHz | | 75 | | dB |

NOTES:

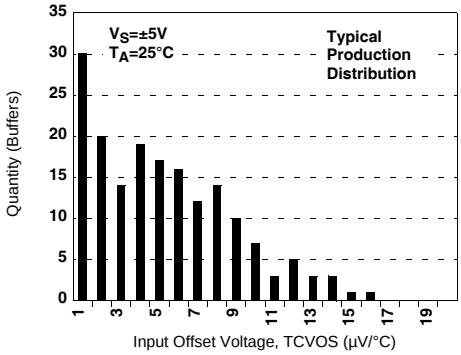
1. Measured over the operating temperature range.
2. Slew rate is measured on rising and falling edges.
3. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

## Typical Performance Curves

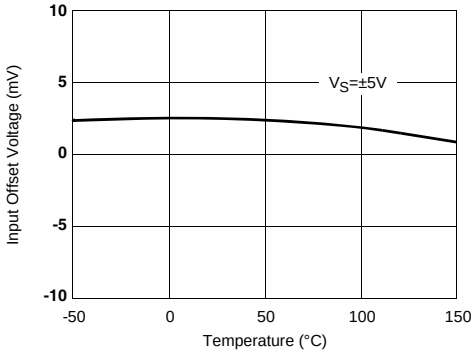
**Input Offset Voltage Distribution**



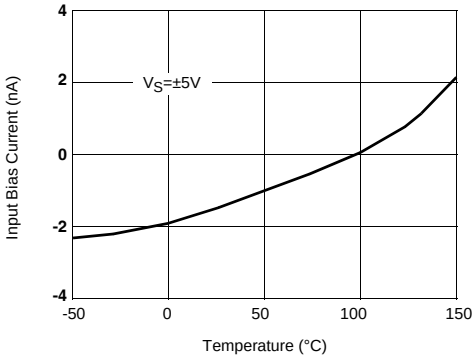

**Input Offset Voltage Drift**



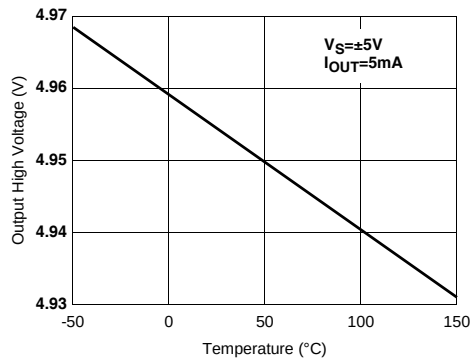

**Input Offset Voltage vs Temperature**



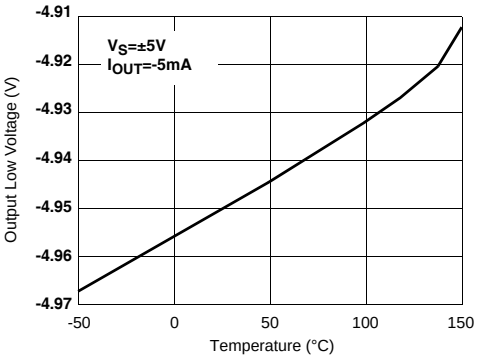

**Input Bias Current vs Temperature**




**Output High Voltage vs Temperature**

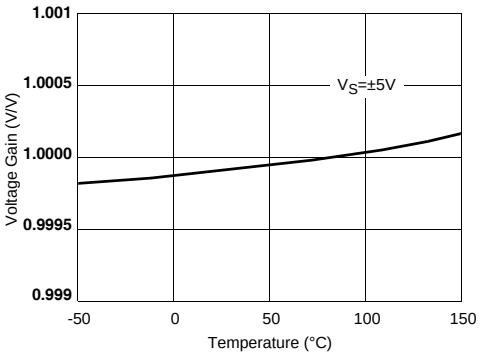



**Output Low Voltage vs Temperature**

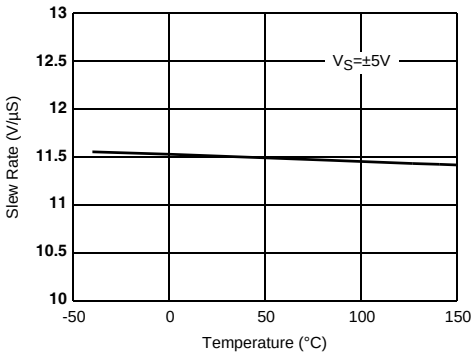


## Typical Performance Curves (Continued)

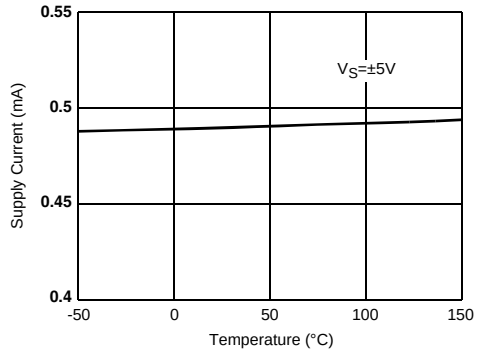
**Voltage Gain vs Temperature**



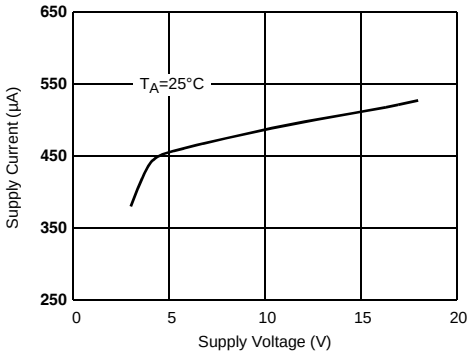

**Slew Rate vs Temperature**



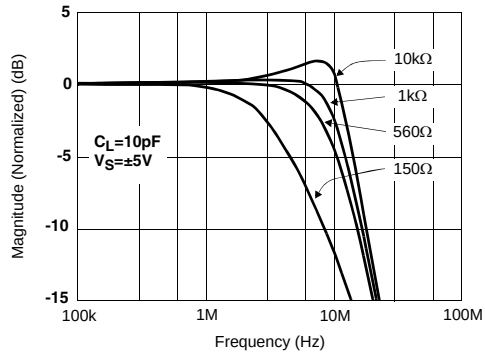

**Supply Current per Channel vs Temperature**



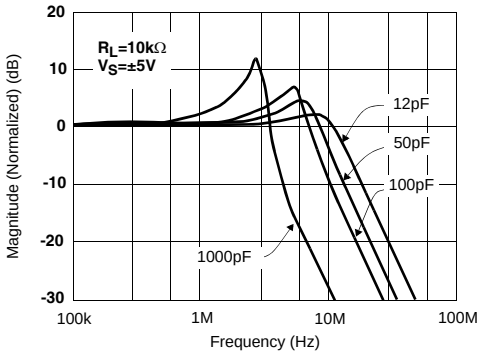

**Supply Current per Channel vs Supply Voltage**




**Frequency Response for Various $R_L$**

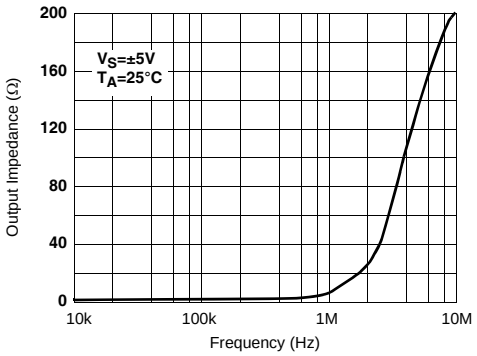



**Frequency Response for Various $C_L$**

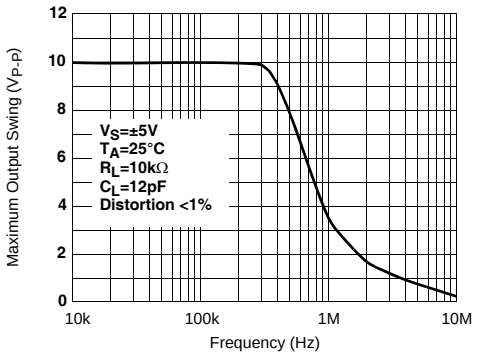


## Typical Performance Curves (Continued)

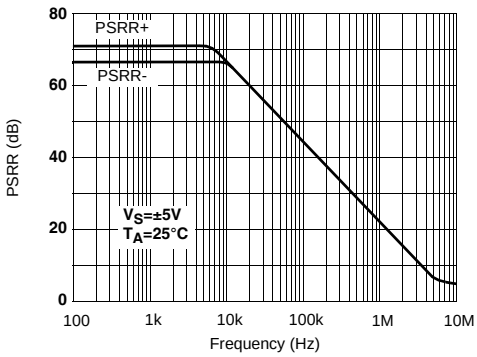
**Output Impedance vs Frequency**



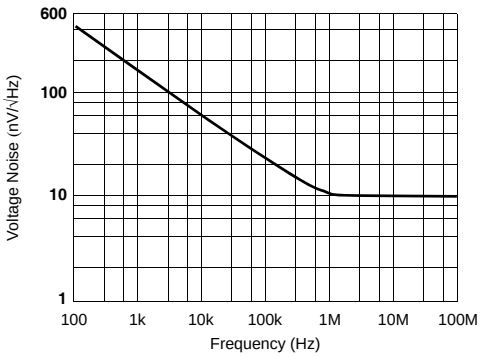

**Maximum Output Swing vs Frequency**



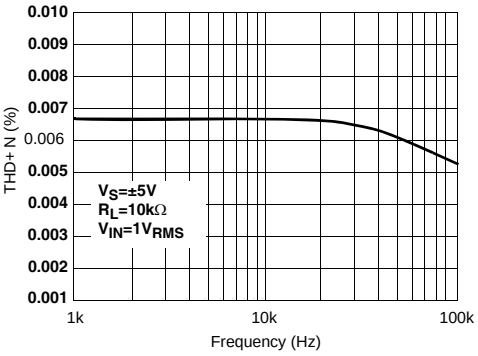

**PSRR vs Frequency**



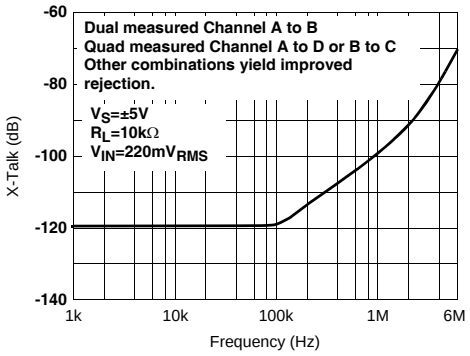

**Input Voltage Noise Spectral Density vs Frequency**




**Total Harmonic Distortion + Noise vs Frequency**

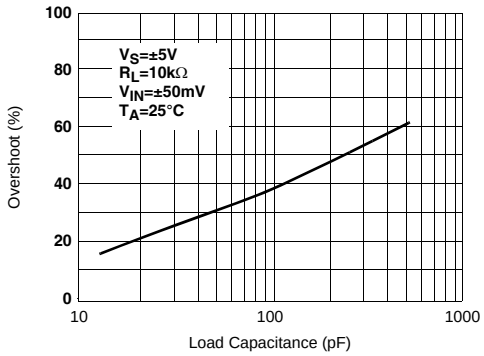



**Channel Separation vs Frequency Response**

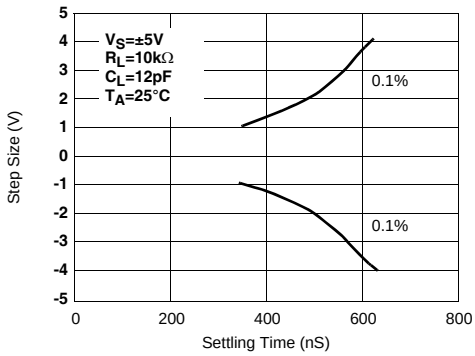


## Typical Performance Curves (Continued)

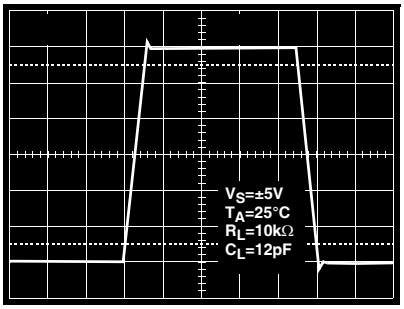
**Small-Signal Overshoot vs Load Capacitance**



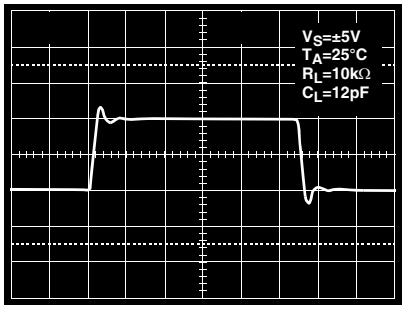

**Settling Time vs Step Size**



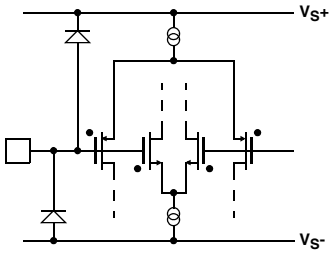
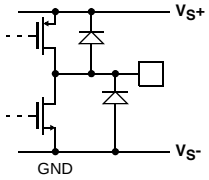

**Large Signal Transient Response**




**Small Signal Transient Response**



## Pin Descriptions

| 6 LD SOT-23 | 8 LD MSOP | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|---|
| 1 | 3 | VINA | Buffer A Input |  Circuit 1 |
| 2 | 4 | VS- | Negative Supply Voltage | |
| 3 | 5 | VINB | Buffer B Input | (Reference Circuit 1) |
| 4 | 7 | VOUTB | Buffer B Output |  Circuit 2 |
| 5 | 8 | VS+ | Positive Supply Voltage | |
| 6 | 1 | VOUTA | Buffer A Output | (Reference Circuit 2) |

## Applications Information

### Product Description

The EL5221 unity gain buffer is fabricated using a high voltage CMOS process. It exhibits rail-to-rail input and output capability and has low power consumption (500µA per buffer). These features make the EL5221 ideal for a wide range of general-purpose applications. When driving a load of 10kΩ and 12pF, the EL5221 has a -3dB bandwidth of 12MHz and exhibits 10V/µs slew rate.

### Operating Voltage, Input, and Output

The EL5221 is specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5221 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The output swings of the EL5221 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 1 shows the input and output waveforms for the device. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.985V_{P-P}$.

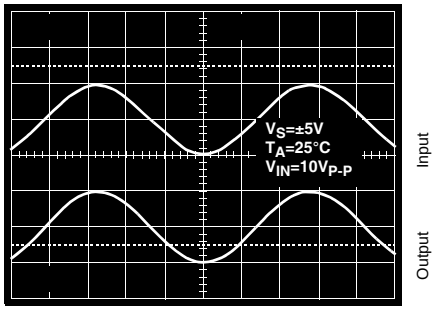



**FIGURE 1. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT**

### Short Circuit Current Limit

The EL5221 will limit the short circuit current to ±120mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±30mA. This limit is set by the design of the internal metal interconnects.

### Output Phase Reversal

The EL5221 is immune to phase reversal as long as the input voltage is limited from $V_S$- -0.5V to $V_S$+ +0.5V. Figure 2 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by

more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

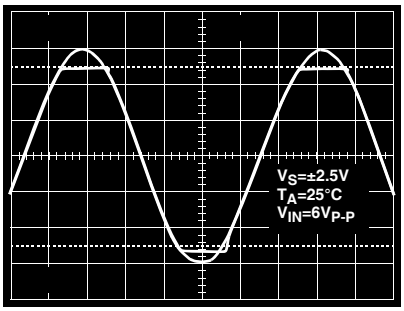



**FIGURE 2. OPERATION WITH BEYOND-THE-RAILS INPUT**

### *Power Dissipation*

With the high-output drive capability of the EL5221 buffer, it is possible to exceed the +125°C “absolute-maximum junction temperature” under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

where:

$T_{JMAX}$ = Maximum junction temperature

$T_{AMAX}$ = Maximum ambient temperature

$\Theta_{JA}$ = Thermal resistance of the Package

$P_{DMAX}$ = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT}i) \times I_{LOAD}i] \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S -) \times I_{LOAD}i] \quad \text{(EQ. 3)}$$

when sinking.

where:

i = 1 to 2 for dual buffer

$V_S$ = Total supply voltage

$I_{SMAX}$ = Maximum supply current per channel

$V_{OUT}i$ = Maximum output voltage of the application

$I_{LOAD}i$ = Load current

If we set the two $P_{DMAX}$ equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. Figure 3 and Figure 4 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if $P_{DMAX}$ exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figure 3 and Figure 4.

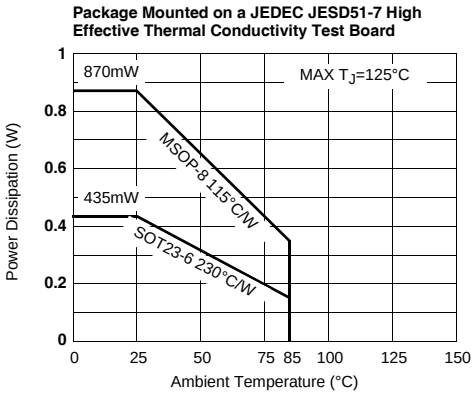



**FIGURE 3. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE**

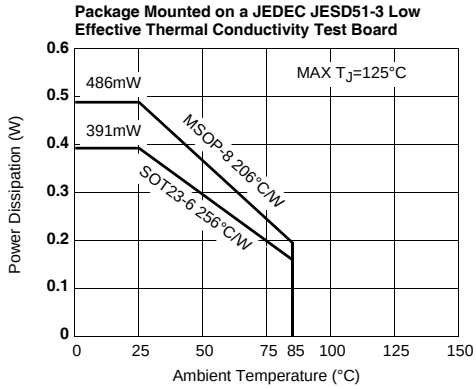



**FIGURE 4. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE**

### Unused Buffers

It is recommended that any unused buffer have the input tied to the ground plane.

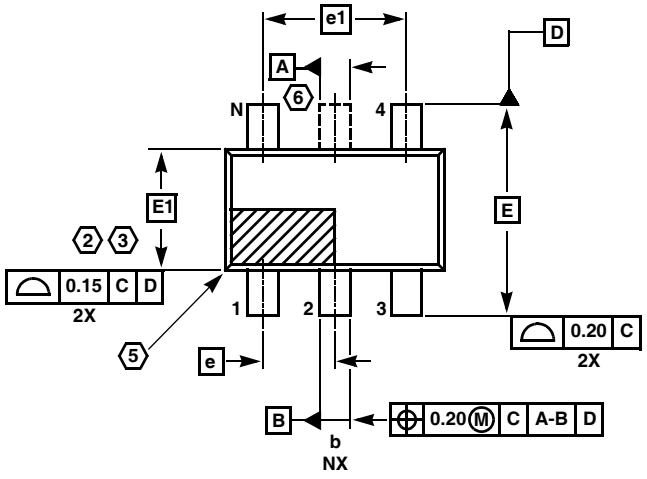
### Driving Capacitive Loads

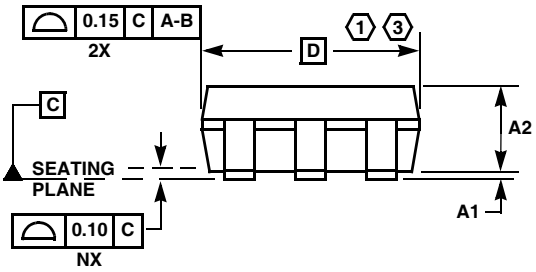
The EL5221 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The buffers drive 10pF loads in parallel with 10kΩ with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain

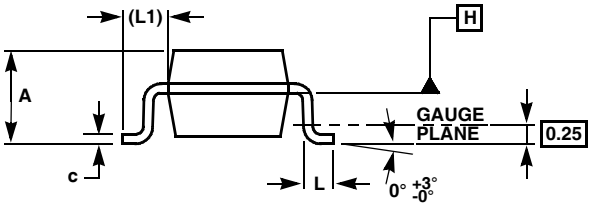
### Power Supply Bypassing and Printed Circuit Board Layout

The EL5221 can provide gain at high frequency. As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the $V_S$- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from $V_S$+ to pin to $V_S$- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the buffer. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

## SOT-23 Package Family




### MDP0038

**SOT-23 PACKAGE FAMILY**

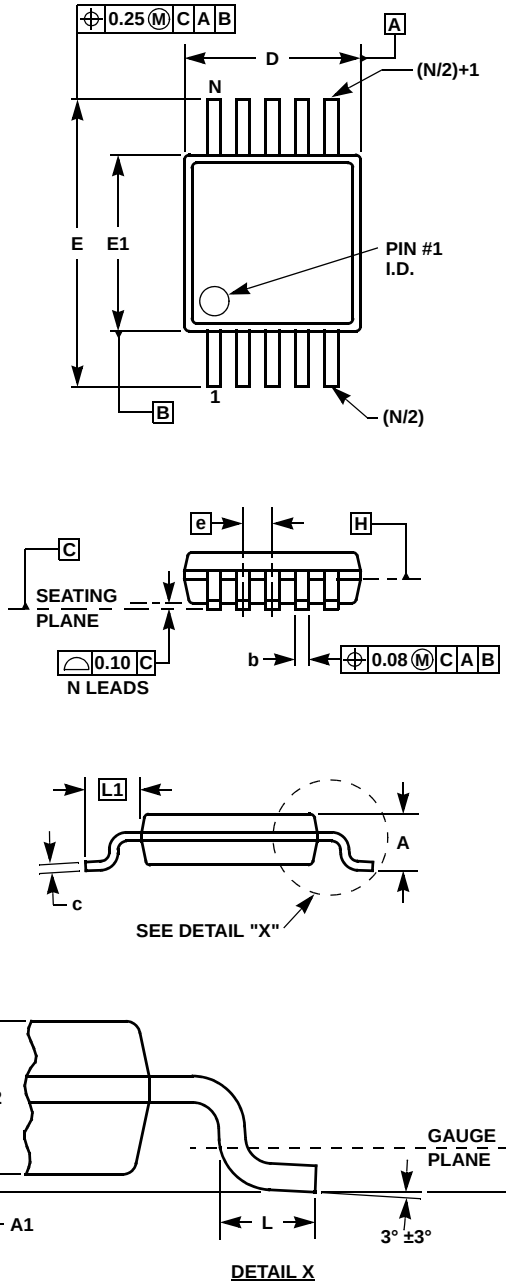
| SYMBOL | MILLIMETERS | | TOLERANCE |
|---|---|---|---|
| | SOT23-5 | SOT23-6 | |
| A | 1.45 | 1.45 | MAX |
| A1 | 0.10 | 0.10 | ±0.05 |
| A2 | 1.14 | 1.14 | ±0.15 |
| b | 0.40 | 0.40 | ±0.05 |
| c | 0.14 | 0.14 | ±0.06 |
| D | 2.90 | 2.90 | Basic |
| E | 2.80 | 2.80 | Basic |
| E1 | 1.60 | 1.60 | Basic |
| e | 0.95 | 0.95 | Basic |
| e1 | 1.90 | 1.90 | Basic |
| L | 0.45 | 0.45 | ±0.10 |
| L1 | 0.60 | 0.60 | Reference |
| N | 5 | 6 | Reference |

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

## Mini SO Package Family (MSOP)




### MDP0043

**MINI SO PACKAGE FAMILY**

| SYMBOL | MILLIMETERS | | TOLERANCE | NOTES |
|---|---|---|---|---|
| | MSOP8 | MSOP10 | | |
| A | 1.10 | 1.10 | Max. | - |
| A1 | 0.10 | 0.10 | ±0.05 | - |
| A2 | 0.86 | 0.86 | ±0.09 | - |
| b | 0.33 | 0.23 | +0.07/-0.08 | - |
| c | 0.18 | 0.18 | ±0.05 | - |
| D | 3.00 | 3.00 | ±0.10 | 1, 3 |
| E | 4.90 | 4.90 | ±0.15 | - |
| E1 | 3.00 | 3.00 | ±0.10 | 2, 3 |
| e | 0.65 | 0.50 | Basic | - |
| L | 0.55 | 0.55 | ±0.15 | - |
| L1 | 0.95 | 0.95 | Basic | - |
| N | 8 | 10 | Reference | - |

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.